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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/726,723	12/03/2003	James S. Zeng	24317/82801	6366

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EXAMINER	
RILEY, SHAWN	

ART UNIT	PAPER NUMBER
2838	

DATE MAILED: 03/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/726,723	ZENG ET AL.	
	Examiner	Art Unit	
	Shawn Riley	2838	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *dec 03 filing*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,9-11,17-23 and 27-29* is/are rejected.

7)☒ Claim(s) *6-8,12-16,and 24-26* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *dec03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to because figure(s) 1-3 fail(s) to have the label prior art. Correction is required.

Specification

Applicant(s) is(are) reminded of the proper content of an abstract of the disclosure. The abstract should not refer to purported merits (**thereby reducing the ripple in the output voltage**) or speculative applications of the invention and should not compare the invention with the prior art. Correction is required. See MPEP § 608.01(b).

Claim Rejections - 35 U.S.C. § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

2. Claims 1-5, 9-11, 17-23, 27-29 are rejected under 35 U.S.C. §102(a) as being fully anticipated by Meng et al. (U.S. Patent 6,512,411). Meng et al. show,[1] (in, e.g., the(ir) figure(s) 3 and corresponding disclosure)

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1 Note claims will be addressed individually and the material in parentheses are the examiner's annotated comments. Further unless needed for clarity reasons, recited limitation(s), will be annotated only upon their first occurrence. Annotated claims begin with the phrase "As to claim". Claims that are not annotated are seen as having already had the invention(s) addressed previously in an annotated claim. For

As to claim 1;

A power control circuit comprising: a switch array comprising: switches (40), a flying capacitor (24-26); and an output voltage terminal (22), capable of providing an output voltage (OUT at 22); a feedback loop (into, e.g., 16) coupled to the output voltage terminal; and a voltage regulator block (including 32/34/36/38), coupled to the feedback loop and to the switch array, the voltage regulator block configured to regulate the output voltage, wherein at least one of the switches is a segmented switch (as stated at column 5 lines 15-21, the arrays are segmented switches-e.g., 30a and 30b,) comprising more than one switch-segment (also as stated at column 5 lines 15-21 the segmented switches contain more that one switch-segment 30a-30i).

As to claim 2;

The control circuit of Claim 1, wherein the switch-segments of a segmented switch (e.g., 30a and 30b) in figure 4a, e.g.,) comprise first and second terminals, wherein the first terminals of the switch-segments are coupled to a first shared rail (both 30a and 30b are connected to, via 30c and 30d, the rail shared by C_1 and C_2); and the second terminals of the switch-segments are coupled to a second shared rail (V_{IN}).

As to claim 3;

The control circuit of Claim 2, wherein the switch-segments have open and closed switching states, wherein the conductance between the first and the second shared rail

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method claims, note that under MPEP 2112.02, the principles of inherency, if a prior art device, in its normal and usual operation, would necessarily perform the method claimed, then the method claimed will be considered to be anticipated by the prior art device. When the prior art device is the same as a device described in the specification for carrying out the claimed method, it can be assumed the device will inherently perform the claimed process. In re King, 801 F.2d 1324, 231 USPQ 136 (Fed. Cir. 1986). Therefore the previous rejections based on the apparatus will not be repeated.

increases when the number of closed switch-segments between the first shared rail and the second shared rail increases (this occurs when, e.g., both 30a and 30b are open, the conductance between them and the rails as described in claim 2 increases).

As to claim 4;

The control circuit of Claim 1, wherein the switch-segments of a segmented switch are organized into switch-segment groups, wherein the switch-segment groups can be labeled so that the number of switch- segments in the switch-segment groups are related to each other as increasing powers of two (labeling **can be** done, and increasing as powers of two **can also be** done).

As to claim 5;

The control circuit of Claim 1, wherein the switch-segments comprise transistors, wherein the transistors are selected from the group of bipolar junction transistors and MOS-FETS (these arrays are made of transistors which are either bipolar or mos type).

As to claim 9;

The control circuit of Claim 1, wherein the voltage regulator block is a digital voltage regulator block (see, e.g., figure 2 and element 28).

As to claim 10;

The control circuit of Claim 9, wherein the digital voltage regulator block is configured to regulate at least one of the switch-segments of at least one segmented switch (see, e.g., column .

As to claim 11;

The control circuit of Claim 9, the digital voltage regulator block comprising: an Analog-to-Digital converter (36); and an encoder (34), coupled to the Analog-to-Digital converter (36), configured to generate a digital error signal from the difference of a reference voltage (42) and a feedback voltage (OUT), provided by the feedback loop.

As to claim 17;

The control circuit of Claim 1, wherein the control circuit is configured to operate at a constant frequency (regulator operates at a constant frequency).

18. A power control circuit, comprising: a voltage supply; a switch may, configured to receive a supply voltage from the voltage supply, comprising: switches; at least one capacitor; and an output voltage terminal; a feedback loop, coupled to the output voltage terminal; and a digital voltage regulator block, coupled to the feedback loop, to the voltage supply, and to the switch array, the digital voltage regulator block configured to 1 1 regulate the supply voltage by digital regulating signals.
19. The control circuit of Claim 18, the switches comprising segmented switches, wherein the digital voltage regulator block regulates the segmented switches.

As to claim 20;

A power control circuit, comprising: a switch array comprising: switches, a flying capacitor; and an output voltage terminal, capable of providing an output voltage, a feedback loop, coupled to the output voltage terminal; and a voltage regulator block, coupled to the feedback loop and to the switch array, the voltage regulator block configured to regulate the output voltage, wherein the power control circuit is operable in charging and pumping phases; and a ripple (see, e.g., column 11 lines 22-25) of the output voltage is controlled both in the charging and the pumping phase.

As to claim 21;

A power control circuit, comprising: a voltage supply; a switch array, configured to receive a supply voltage from the voltage supply, comprising: switches; at least one capacitor; and an output voltage terminal; a feedback loop, coupled to the output voltage terminal; and a voltage regulator block, coupled to the feedback loop, to the voltage supply, and to the switch array, the voltage regulator block configured to regulate the supply voltage, wherein the power control circuit does not include a pass transistor (Meng et al. do not discuss a pass transistor).

22. A method of controlling an output voltage of a power control circuit, the method comprising: generating an output voltage at an output voltage terminal of the power control circuit; generating a feedback voltage by feeding the output voltage back to a voltage regulator block by a feedback loop; and regulating the output voltage according to the feedback voltage by the voltage regulator block controlling at least one segmented switch of a switch array.
23. The method of Claim 22, wherein regulating the output voltage comprises generating a digital error signal by an Analog-to-Digital converter and a coupled encoder from the difference of a reference voltage and the feedback voltage.
27. A method of controlling an output voltage of a power control circuit, the method comprising: providing a supply voltage by a voltage supply to a switch array; generating an output voltage at an output voltage terminal; generating a feedback voltage by feeding the output voltage back to a digital voltage regulator block by a feedback loop; and
regulating the output voltage by the digital voltage regulator block digitally controlling at least one switch of the switch array according to the feedback voltage.
28. The method of Claim 27, wherein at least one of the switches comprises at least one segmented switch.
29.A method of controlling an output voltage of a power control circuit, the method comprising: providing a power control circuit, comprising: a switch array comprising: switches; a flying capacitor; and an output voltage terminal, capable of providing an output voltage; a feedback loop, coupled to the output voltage terminal; and a voltage regulator block, coupled to the feedback

loop and to the switch array, the voltage regulator block configured to regulate the output voltage; operating the power control circuit in charging and pumping phases; and controlling a ripple of the output voltage both in the charging and the pumping phase.

Allowable Subject Matter

3. Claims 6-8, 12-16, and 24-26 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

4. As allowable subject matter has been indicated, applicant's response must either comply with all formal requirements or specifically traverse each requirement not complied with. See 37 C.F.R. § 1.111(b) and section 707.07(a) of the M.P.E.P.

5. The following is an examiner's statement of reasons for allowance: No prior art uncovered anticipates or renders obvious applicant(s) claimed method or circuit of regulating the output voltage having generating an add-subtractor signal by performing an arithmetic operation by an add-subtractor on the digital error signal and a sample-and-hold gate signal.

Further, no prior art uncovered anticipates or renders obvious applicant(s) claimed control circuit having a fourth switch is coupled between the fourth switch node and a fifth switch node, wherein the first and third switches are capable of assuming a first switching state, and the second and fourth switches are capable of assuming a second switching state, wherein the first and second switching states are opposite.

Conclusion

Any inquiry from other than the applicant/attorney of record concerning this communication or earlier communications from the Examiner should be directed to the Patent Electronic Business Center (EBC) at 1.866.217.9197. Any inquiry from a member of the press concerning this communication or earlier communications from the Examiner or the application should be directed to the Office of Public Affairs at 703.305.8341. Any inquiry from the applicant or an attorney of record concerning this communication or earlier communications from the Examiner should be directed to Examiner Riley whose telephone number is 571.272.2083. The Examiner can normally be reached Monday through Thursday from 7:30-6:00 p.m. Eastern Standard Time. The Examiner's Supervisor is Mike Sherry who can be reached at 571.272.2084. Any inquiry about a case's location, retrieval of a case, or receipt of an amendment into a case or information regarding sent correspondence to a case **should be directed to 2800's Customer Service Center** at 571.272.2815. Any papers to be sent by fax MUST BE sent to fax number 703.872.9306. Any inquiry of a general nature of this application should be **directed to the Group receptionist** whose telephone number is 571.272.2800. Status information of cases may be found at http://pair-direct.uspto.gov wherein unpublished application information is found through private PAIR and published application information is found through public PAIR. Further help on using the PAIR system is available at 1.866.217.9197 (Electronic Business Center).

March 05

Shawn Riley
Primary Examiner